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A low voltage 8-bit digital-to-analog converter using floating gate MOSFETs

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Abstract A new low voltage digital-to-analog conversion (DAC) architecture is proposed using weighted summation of voltages at the input terminals of a Floating Gate MOSFET (FGMOS). An 8-bit DAC has been designed based on this architecture and its simulation results are provided to verify its operation at ±1.0 V. The circuit possesses good accuracy, fast dynamic performance and low power consumption. The circuit operation was verified through SPICE simulations carried out using 0.13 μm CMOS technology.

Keywords Digital-to-analog converter (DAC) · Floating gate MOSFET · Low voltage mixed-signal circuits · Low power circuits

1 Introduction

The development of complex structures for Systems on Chip (SoC) architecture is increasingly becoming dependent on compact mixed-signal systems, embedding high performance analog blocks with complex digital circuitry on the same chip. This necessitates the design of small and simple DACs. Unfortunately, to achieve an acceptable resolution and good performance, a considerable amount of complexity and silicon area is required. Power consumption is also a dominant factor in IC design [1].

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The design of DACs based on standard CMOS technologies has been pursued to overcome these constraints with some success [2–7]. Although each of the converters have some attractive features, in the form of either consuming low power [2–5], or possessing good dynamic performance [6], all of them consist of segmented or matrix architecture, rendering a complexity to the D/A converter circuit.

In this paper, a novel topology to design DACs by exploiting the ability of Floating Gate MOSFET (FGMOS) [8], a device introduced in the last decade and used frequently in digital designs, to achieve a weighted sum of input voltages is presented. Though D/A conversion through FGMOS can also be obtained using different approaches such as programming of floating gate charge [9, 10], etc., the resultant DAC is relatively complicated. The proposed circuit shows good accuracy and dynamic performance and its simple architecture and low power consumption make it quite promising for integration.

2 FGMOS transistor

An n-input FGMOS transistor consists of a gate electrode which is left electrically floating. This floating gate is capacitively coupled to an array of n control gates through a second polysilicon layer. The terminal voltages and various capacitive coupling coefficients are defined in Fig. 1(b), where V_{FG} is the floating gate potential, V_1, $V_2 \ldots V_n$ are the input signal voltages and C_1, $C_2 \ldots C_n$ are the capacitive coupling coefficients between the floating gate and each of the input gates.

Let Q_{FG} denote the net charge on the floating gate, which is calculated as

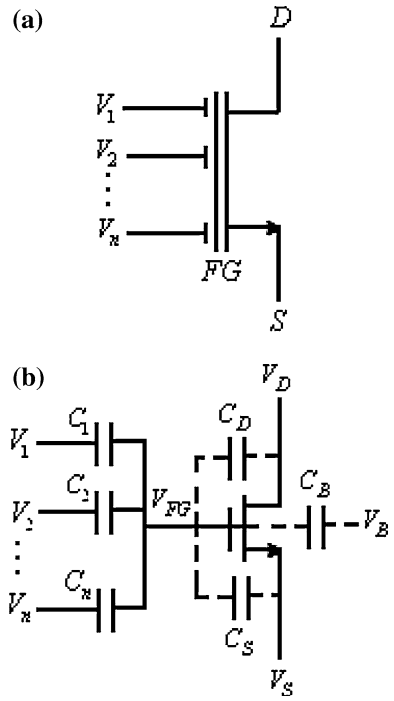

Fig. 1 FGMOST (**a**) Symbol (**b**) Equivalent circuit

$$Q_{FG} = \sum_{i=1}^{n}(V_i - V_{FG})C_i + (V_S - V_{FG})C_S + (V_D - V_{FG})C_D + (V_B - V_{FG})C_B \quad (1)$$

where C_S, C_D and C_B are the parasitic capacitances between gate and source, drain and body, respectively. V_S, V_D and V_B are the potentials at the respective terminals.

Under normal circumstances, Q_{FG} is equal to the initial charge on the floating gate, which is assumed to be zero in this case for simplicity. Then Eq. 1 reduces to

$$V_{FG} = \frac{\sum_{i=1}^{n} C_i V_i + C_S V_S + C_D V_D + C_B V_B}{\sum_{i=1}^{n} C_i + C_S + C_D + C_B} \quad (2)$$

Since C_S, C_D and C_B are quite small in comparison to the capacitive coefficients, C_i, Eq. 2 can be safely approximated to

$$V_{FG} \approx \sum_{i=1}^{n} k_i V_i \quad (3)$$

where $k_i = C_i/C_{Total}$ and

$$C_{Total} \approx \sum_{i=1}^{n} C_i \quad (4)$$

3 Principle of operation and design

The proposed approach for the design of the n-input DAC is explained through the circuit structure shown in Fig. 2.

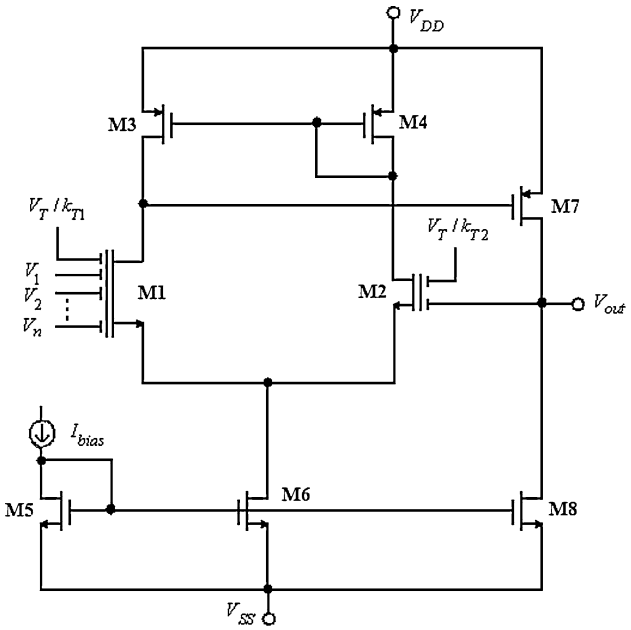

Fig. 2 Proposed n-bit DAC

Transistors M1 and M2 are multiple input floating gate MOSFETs (MIFG) with n and two gate inputs, respectively.

Now V_{FG1}, the floating gate potential of M1, can be written as

$$V_{FG1} \approx \sum_{i=1}^{n} k_i V_i + k_{T1}\left(\frac{V_T}{k_{T1}}\right) \quad (5)$$

where $k_{T1} = C_{T1}/C_{Total1}$, C_{T1} and C_{Total1} being the capacitive coupling coefficient of the topmost control gate of M1 and total capacitance of M1, respectively, and V_T is the threshold voltage of M1 and M2.

As M1 and M2 form a differential pair, $V_{FG1} \approx V_{FG2}$

$$V_{FG2} \approx k_o V_{out} + k_{T2}\left(\frac{V_T}{k_{T2}}\right) \approx \sum_{i=1}^{n} k_i V_i + k_{T1}\left(\frac{V_T}{k_{T1}}\right) \quad (6)$$

where V_{FG2} is the floating gate potential of M2, $k_{T2} = C_{T2}/C_{Total2}$ and $k_o = C_o/C_{Total2}$, C_{T2}, C_o and C_{Total2} being the capacitive coupling coefficients of the respective control gates of M2 and total capacitance of M2, respectively.

Equation 6 can be simplified as

$$V_{out} \approx \frac{1}{k_o}\sum_{i=1}^{n} k_i V_i \quad (7)$$

Or,

$$V_{out} \approx \frac{1}{k_o C_{Total1}}\sum_{i=1}^{n} C_i V_i \quad (8)$$

If the die is designed to have

$$C_i = \frac{C_{FG}}{2^i} \tag{9}$$

then Eq. 8 becomes

$$V_{out} \approx \frac{C_{FG}}{k_o C_{Total1}} \sum_{i=1}^{n} \frac{V_i}{2^i} \tag{10}$$

where C_{FG} is the common factor with a suitable value.

4 Low voltage D/A converter

The structure of DAC shown in Fig. 2 has been modified by using a low voltage current mirror proposed in [11], and the resultant circuit for the low voltage D/A converter (LV DAC) is shown in Fig. 3. To drive M3 in saturation, M6 is biased in sub-threshold region by selecting I_{bias1} at sufficiently low level. M6 acts as a level shifter, reducing the minimum voltage drop across the current mirror. This arrangement reduces the power supply requirements of the D/A converter, thereby reducing the power consumption.

5 Simulation results

SPICE simulations using 0.13 μm CMOS technology were carried out to validate the operation of both the DAC circuits and evaluate their performance characteristics [12]. The simulations were run at 100 M samples/s.

It may be noted that application of inputs V_T/k_{T1} and V_T/k_{T2} at the gates M1 and M2, respectively, is optional. But it was found through simulation that application of

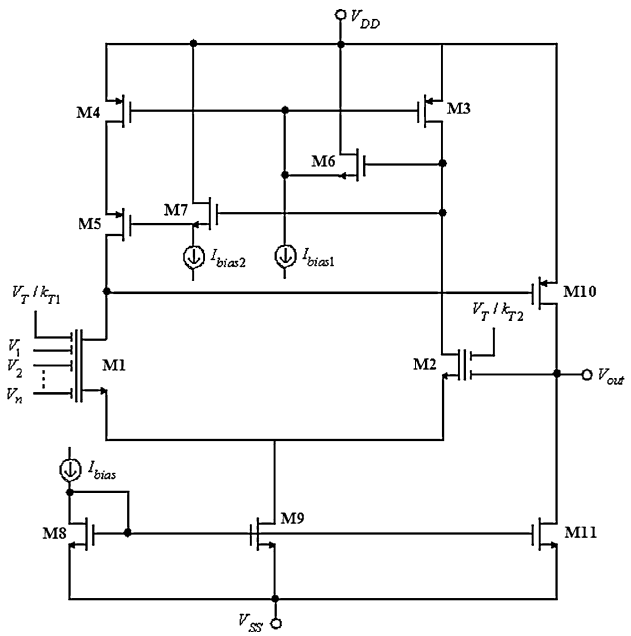

Fig. 3 Proposed *n*-bit low voltage DAC

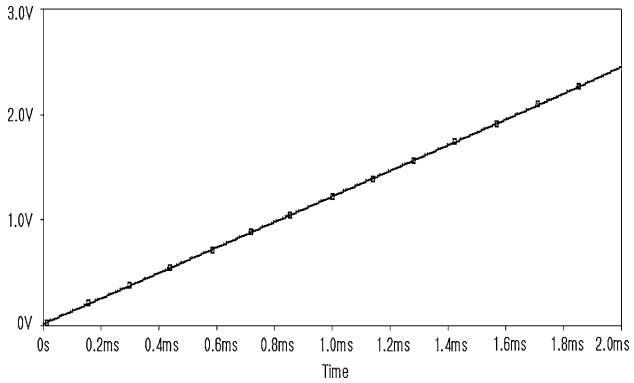

Fig. 4 DAC output voltage

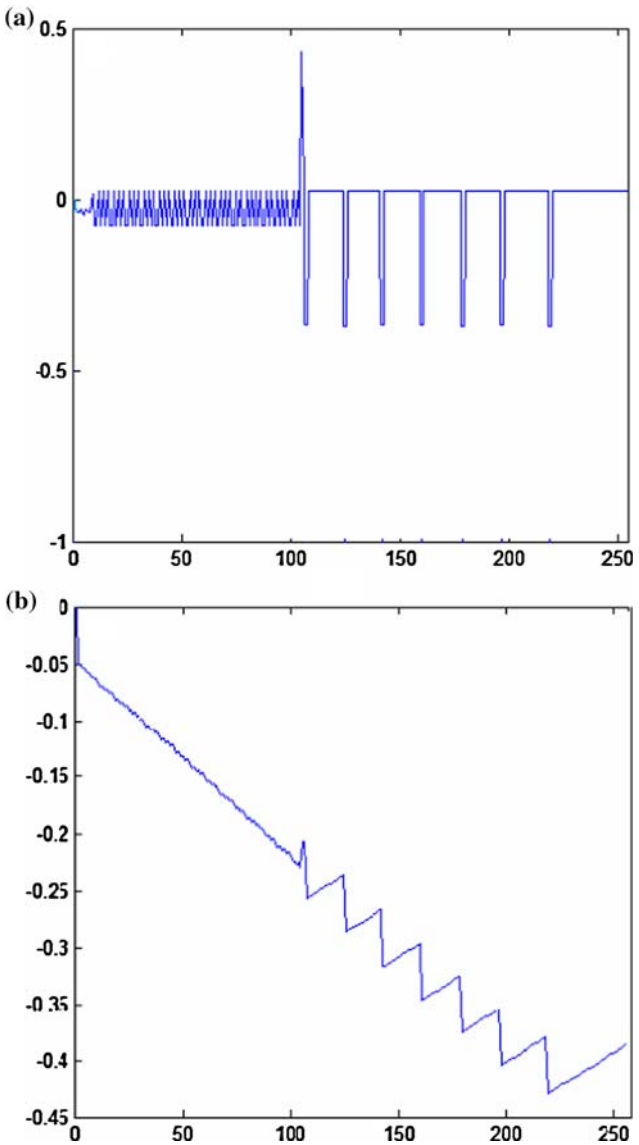

Fig. 5 Static performance of DAC (**a**) Differential non-linearity (**b**) Integrated non-linearity

Table 1 Summary of simulation results

Parameters	DAC	LV DAC
Process (μm CMOS)	0.13	0.13
Supply voltage (V)	±2.5	±1
Update rate (MS/s)	100	100
Resolution (bit)	8	8
Full scale range (V)	2.42	0.92
LSB (V)	0.009765625	0.00390625
DNL	0.43 LSB	0.5 LSB
INL	0.43 LSB	0.5 LSB
SFDR (F_s = 100 MHz) (dB)	59	58
Power dissipation (mW)	1.45	0.561

these two inputs removes the transition glitches that were found to be present in the circuit's response, thereby reducing the static non-linearities.

5.1 Proposed DAC

The circuit was operated at a power supply voltage of ±2.5 V, whereas digital LOW and HIGH voltage levels were 0 and 1.5 V and I_{bias} was 100 μA. The output response for the 8-bit DAC is shown in Fig. 4. As seen in Fig. 5, a good accuracy is achieved, and the performance parameters INL and DNL were found to be around 0.43 LSB each. The circuit was found to possess an offset error of 25.22 mV and a full scale gain error of 0.071 V. Simulated values of other performance indices are presented in Table 1.

5.2 LV DAC

The DC output voltage and static linearities for an 8-bit LV DAC are shown in Figs. 6 and 7, respectively. The LV DAC can be operated at a power supply voltage of ±1 V, with the digital LOW and HIGH voltage levels being 0 and 0.5 V. The bias currents, I_{bias1}, I_{bias2} and I_{bias3}, were set at 10 nA, 20 μA and 100 μA, respectively. The INL and DNL for this circuit have been found to be 0.5 LSB. A comparison of its simulated performance with the proposed DAC is provided in Table 1.

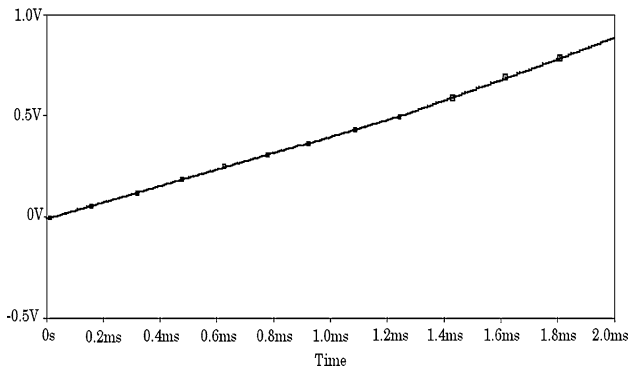

Fig. 6 LV DAC output voltage

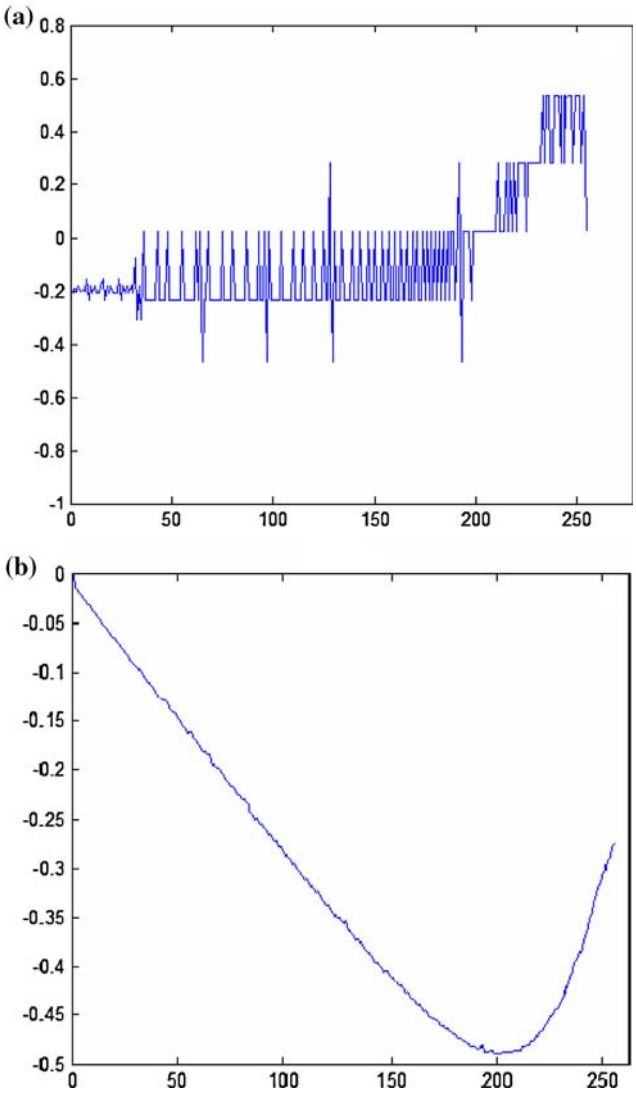

Fig. 7 Static performance of LV DAC (**a**) Differential non-linearity (**b**) Integrated non-linearity

6 Conclusion

A new D/A conversion circuit architecture using floating gate MOSFETs has been presented. The scheme exploits the property of weighted summation of gate-voltages, with capacitive coupling ratios as weighting coefficients. The proposed structure possesses good accuracy and low power consumption which have been verified using SPICE simulations of 8-bit version. The power consumption and supply requirements can be further compressed by employing a low voltage current mirror, without much effect on the performance. Due to their simple structures, the proposed DACs are suitable for complex on-chip mixed-signal circuit blocks.

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